Design and Development of Application-Specific FPGA/Reconfigurable Hardware Generator

The project aimed to design a GUI (Graphical User Interface)-based software platform which can be used to design, explore and generate application-specific FPGA and similar reconfigurable architectures. These alternate FPGA (reconfigurable) architectures were optimized for target applications in terms of area, speed and/or power consumption. The output of this tool was VHDL files of the optimized FPGA architecture which were translated into GDSII format files for fabrication using third-party tools. This platform also mapped application circuits on the architecture through advanced mapping algorithms and generated their bitstreams (binary files). These application circuits encompassed fields as diverse as data and telecommunication, security, multimedia, medical, and other real-time Digital Signal Processing (DSP) systems.

Key Objectives

- Develop an exploration environment to explore five different reconfigurable architectures. This exploration environment is named as VERA (Visual Explorator for Reconfigurable Architectures)
- Automatically generate VHDL codes of all the reconfigurable architectures supported by the exploration environment (VERA).
- Develop a Graphical User Interface (GUI) to visualize different architecture features of Reconfigurable Architectures.
- Write/gather different test bench circuits to test the proposed reconfigurable architectures.
- Consolidate embedded Systems research group at KIET.
- Design specialized research courses for graduate program at KIET.
- To produce relevant technical work force that can do R&D work on internal architecture design of FPGAs and its CAD tools.
- To publish our research in reputed and relevant conferences and journals.
- To lay the grounds of a start-up CAD tool company.

Significant Results

- Development of an exploration environment to explore different reconfigurable architectures was completed.
    a. **Architecture Exploration**
        i. **Reconfigurable Network on Chip (RNoC)**
        ii. **Regular-ASIF**
        iii. **FPGA-to-ASIC**
    b. **Architecture Comparison**
        i. **Area comparison**
        ii. **Delay comparison**
        iii. **ASIF vs FPGA**
    c. **Architecture optimization**
        i. **Optimized mapping of application on ASIF**
        ii. **Area optimization**
        iii. **Delay optimization:**
            1. Circuit Delay was optimized by
                a. Compromising the flexibility of routing network.
                b. Reducing the area of overall architecture.
            2. CAD run-time was reduced by
                a. Proposing optimization in Placement algorithm Proposing

optimization in Routing algorithm.

- Development of an HDL generator that can automatically generate VHDL descriptions for 5 different reconfigurable architectures was completed.
- Development of a Graphical User Interface to be attached on top of VERA was completed.
- Development of important test bench circuits to test the performance of the proposed architectures was completed.
- 2 International Journal publications (under review) and 3 International conference paper published at renowned conferences.
- 1 National conference paper published and 1 National conference publication (under review).
- As part of the process, we learnt a great deal with the reviews which accompanied both with the acceptance and rejection of our manuscripts sent to various conferences and journal papers.
- 1 MS thesis successfully defended (Ali Asghar) and 1 PhD thesis student (M. Mazhar Iqbal) still continuing work on the research-tasks of the ICTRnD project.
- 3 MS thesis students (Baqar, Faisal Riaz, Ameen) will soon defend their MS thesis concerning the research-tasks of the ICTRnD project.
- 4 MS students (not paid through this project) (Maarij, Adeel Amin, Faisal Din, Ali Umair) actively continuing MS thesis work with Embedded Systems Research Group at KIET whereas many other students are in the process of starting their thesis with Embedded Systems research group.
- As part of process, there is a long list of students who started work with Embedded Systems group, but left us earlier before achieving some significant results.
- Three graduate level courses designed and actively taught at KIET are:
    - Reconfigurable Computing
    - Advanced Computer Architecture
    - FPGA-based Systems Design.

There were also achievements made in national and international level, listed below:

- Embedded systems group in collaboration with Signal Processing group at KIET won an ICTRnD project on the design of an FPGA-based Face recognition system. The project is funded with approximately 13.8 million Pak Rupees for a time period of 2 years.
- Shortly Embedded Systems group is going to start a related research project in collaboration with University of Umm-al-Qura, Mecca, Saudia Arabia. The project is funded with approximately 2 million Saudi Riyals (i.e. 55.5 million Pak Rupees) for a time period of 2 years.