Massively Parallel Fingerprint Recognition System Architecture For Performing Multi Million Matches Per Second

Start Date: Sept 2008 **Date of completion:** July 2010

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B. Project Summary:

The main objective of this R&D activity was to develop an efficient matching algorithm and system architecture that could be used for designing systems capable of performing multi millions of fingerprint matching per second. Majority of current market solutions capable of providing such speeds in biometric data processing are all software based cluster systems; with major disadvantages of being large complex systems that are quite costly. We aimed to address these main drawbacks by building a solution that was relatively cheaper and easier to manage without compromising on the processing power.

We were able to achieve our goals estimably. The developed matching algorithm is quite accurate in nature and highly efficient. The designed system architecture is scalable in nature, facilitating the attainment of our speed goals. Scalability allows the realization of high speed by using multiple hardware blocks in parallel running similar matching engines; when plugged into a matching server they are able to yield matching speeds in linear multiples.

Initially matching algorithms were researched & developed. Since eventually they were to be implemented in hardware, these algorithms were considered with a particular emphasis on their hardware affinity. The developed matching algorithm was then explored for potential parallelism at different levels. Architecture was designed, characterized and evaluated. High-end FPGA based Commercially Off The Shelf (COTS) boards were used for the implementation of algorithm. The architecture was then coded in Verilog for mapping on to FPGA based systems.

The team executing this project included experienced and otherwise, professionals, engineers and researchers at CARE along with MS and PhD research students from CASE. Besides creating the obvious job opportunities the project facilitated the development of expertise in biometrics and system design.

C. Objectives and achievements

■ Original Project Objectives

Research Objectives:

1. To explore fingerprint matching algorithms and compare their performance and hardware affinity.
2. To develop an algorithm which can be mapped to FPGA-based hardware systems.
3. To design a Fingerprint Matching Processor based on the designed algorithm.
4. To characterize the Fingerprint Matching Processor for the number of matches it can perform in every second.
5. To develop a scalable architecture utilizing multiple instances of the Fingerprint Matching Processor for high density applications.

Academic Objectives:

1. To develop a research group in CASE, working on state of the art algorithms on biometrics in general and fingerprint matching in particular.
2. To strengthen the DSP-Architecture group at CASE that is specialized in mapping signal processing algorithms to silicon.
3. To design a specialized graduate level course focusing on VLSI mapping technique of signal processing algorithms.

Industrial Objectives:

1. To develop a parallel architecture that can be employed in designing high density fingerprint matching systems.
2. To develop algorithms that can be used for software based fingerprint matching applications.
3. To develop the architecture, where other biometric applications like face recognition, palm recognition, and footprint recognition can also be mapped for hybrid biometric systems.

Other Objectives:

1. To develop an infrastructure that can generate some financially rewarding activity.
2. To work as an example for other academic institutions for realizing a marketable research idea.
3. To develop human resource for state of the art algorithm development and architecture design, that can perform the ‘concept to product’ realization.
4. To develop human resource for testing and qualification of high-end systems.

■ **Objectives Achieved**

On the whole this project has been successful in achieving its envisioned goals. The extent to which the individual objectives succeeded are:

1. Fingerprint Matching Algorithms were studied in detail and we were able to develop our own Matching Algorithm which can be mapped to FPGA-based systems.
2. A Fingerprint matching Processor was designed based on the developed algorithm; it is categorized by speed (matches per second) and provides a scalable solution that can be incorporated into higher density systems by using multiple instances of the same.
3. Execution of this project has developed a team individuals significantly experienced in the domain of biometrics with fingerprint matching in particular.
4. The developed architecture is parallel in nature and can be deployed into larger systems by using multiple instances of it.
5. The originally developed algorithms in C can be used in software based matching systems, but with reduced speed outputs.
6. Marketing of this solution will create new opportunities and ultimately be financially rewarding for all entities concerned.
7. Besides generating expertise in biometrics, this project was able to create human resource experienced in architecture design and high end system testing.

D. Technology Transfer/Commercialization Approach

The developed system architecture both in the form of algorithm and architecture are available in soft form. Detailed documentation has been generated for the developed technology. The developed technology will be transferred in the form of IP with associated documentation.

The developed algorithm and architecture can easily be used in other products. The project outputs are sustainable; the algorithms can be directly used in other fingerprint applications. Similarly the Fingerprint Matching Processor can also be used in high-end hardware based systems. The Application Programming Interfaces (APIs) have been provided. Other applications can easily hookup the developed matching algorithm/architecture using these APIs. This is a standard practice used for commercialization where IPs are provided with APIs to be used with other applications.

E. Benefits of the Project

■ Outputs of the project and potential beneficiaries

The fundamental output of this project is an efficient fingerprint matching algorithm that can be used in a variety of applications and a system architecture that allows for performing multi-million matches per second using said algorithm. The designed system architecture being scalable in nature can be used in a multitude of high end systems where speed is a crucial concern. As biometric technology is rapidly becoming the means of verifying identities and logging human information, this project will find a vast array of applications. Potential beneficiaries of this technology are organizations that require swift processing of large amounts of biometric data. Since the developed technology will have an international market the potential customers include:

- Immigration organizations,
- National security agencies,
- Banks,
- National registration agencies etc.

And most specifically National law enforcement agencies, where fingerprint data received from all over the country needs to be searched & matched in a central database.

■ Organizational Outcomes

In addition to creating a group with prolific expertise in biometric technology; the execution of this project has produced excellent human resource able to take on other projects of comparable complexities and scale in the future.

■ National Impacts

Success of this endeavor will pave the way for more organizations to follow suit. This should create more R&D in the field of biometrics and recognition for our country as a destination of progressive biometric technology. And consequently commercial success for this and other such ventures will be able to create an inflow of foreign investment for our country.

F. Assessment of Project Structure

■ Project Team

Everyone associated with this project has performed considerably well. There were no major departures from the proposed structure of the team. The project team consisted of experienced professionals in senior positions as well as lesser experienced individuals in design positions. A number of internees also joined the team from time to time, where some of them were subsequently hired on good performance

■ Collaborations

The main collaborators for this research project were:

1. Centre for Advanced Research in Engineering (**CARE**), through which experienced personnel were involved directly as employees or indirectly as guides to this project, it also provided the organizational structure for execution of this project.
2. College of EME National University of Science and Technology (**NUST**), which was represented by Dr. Shoab A. Khan as one of the directors on the funded project.
3. Centre for Advanced Studies in Engineering (**CASE**), the Principal Investigator, which provided the platform for the execution of the funded project and provided MS and PhD research students from academia to directly contribute to the research endeavors of this project.

G. Research Approach

The main steps performed in this project are as under; the first two steps encountered no major difficulties but the rest are detailed accordingly:

1. Research & Development of an accurate fingerprint matching algorithm
2. Algorithm Implementation & Verification in Matlab.
3. Porting of the Algorithm to Fixed-point C; the only complexity in this step was maintaining the precision of results while using a fixed point implementation
4. Hardware Architecture Exploration and Design; some parts of the designed algorithm were not suitable for hardware portability and subsequently had to be re-designed.
5. Coding of Architecture in Verilog and its functional verification; same as step 3 precision in hardware results was an issue otherwise no major difficulties were encountered in this phase.
6. Synthesis and porting on to FPGA-based COTS boards; the main challenge here was getting the architecture to fit on the available FPGA and meeting its timing, subsequently some portions of the algorithm had to be modified to do so.
7. Incorporation in application and HW-SW co-verification; this was the most challenging phase; difficulties arose in both hardware and software domains and were handled by their respective teams.

The project steps have been carried out as proposed in the application. There were no major departures from the planned approach.

H. Assessment of Project Schedule

This project has been carried out over a period of 23 months. As proposed this project consisted of 6 milestones and their deliverables. The first 5 milestones were completed with their deliverables submitted on time. The last milestone was the conclusion of the hardware software integrated verified design which was delayed due to a number of unavoidable reasons. Due to rupee-dollar parity, the initial budget set aside for recommended FPGA board did not suffice. The procured FPGA boards are the substitute having comparatively less area and memory. Porting of matching algorithm to FPGA became more challenging. Retention of human resource during the course of the project also became one of the main reasons to delay the last milestone. However, the fiasco at National ICT R&D fund over the appointment of the new CEO, removal of the board members and other political pressure affected the project schedule drastically as it left no hopes for the PI for the disbursement of the funds to sustain the project.

I. Assessment of Project Costs

The project has been carried out within the planned budget. As previously mentioned the developed architecture is scalable in nature and greater speed figures can be attained by using larger and consequently more costly hardware resources.