Design and Verification of Low-Power, High-Speed IP Suite for Universal Serial Bus (USB 3.0)

The primary objective of a project was to design a low cost and high speed Host and Device IP solution for SuperSpeed universal serial bus (USB 3.0), which has been achieved successfully.

But beside this implementation objective project have many other objectives too that the team successfully achieved by the end of project.

1. Successfully develop world-class Host and Device IP for the Semiconductor design and development markets.
2. Researched different design and verification techniques for developing high speed IP cores for Speed critical devices.
3. Research objectives were fully achieved and two MS student's thesis that has been carried out on USB 3.0 project.

    - One of MS student thesis was on to the development of macro architecture and the micro-architectures for the Host and Device controllers for SuperSpeed USB.
    - The other student thesis was on low power optimization techniques and to look for their applicability to the proposed design.
    - Project also provides a platform to develop research group that is working on high-speed computer and networking interfaces, it also strengthen the SoC group at NUST.
    - Created a close tie between Academia in Pakistan and companies participating on state-of-the-art Semiconductor IP technology serving international markets.
    - The project also created many internships and job opportunities for undergraduate and graduate students. It also helped to trained undergraduate and graduate students to meet the talent demand for our next R&D center in Pakistan.

Significant achievements:

- Designed USB 3.0 host/ device IP solution is unique and innovative in the sense that it addresses all requirements. In terms of providing the risk free IP solution, the team came up with the complete solution for USB 3.0 host & device that includes the design

& verification platform on simulation level and as well as providing the hardware validation on real USB 3.0 clock speeds with ease of integration into 3rd party products.

- The team also came up with the Patent pending architecture for High Speed Communication Protocol that maximizes the USB 3.0 bandwidths to ideal numbers and meantime minimizes the overall power dissipation.

- The solution is fully xHCI complaint Host/ Device Protocol Layer, Data Link Layer, Host and Device models and complete verification test benches with automated transaction and traffic generators through user specification for USB 3.0. NUST solution also provides complete emulation solution on real USB 3.0 clock speed using the FPGA development boards. The team is planning to certify the USB 3.0 host/device through the USB.org to build customer confidence and to minimize customer risk to zero. Hence customer can run real time traffic using the real hardware through our designed USB 3.0 host and device IP solution.